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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,940	07/03/2003	Menahem Lasser	246/209	5428

7590 08/22/2005

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,940	LASSER, MENAHEM	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,18-35,38-41,44,45 and 47-50* is/are rejected.

7)☒ Claim(s) *14-17, 36-37, 42-43, 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/3/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claims 10, 16-38 and 46-50 are objected to under 37 CFR 1.71 because of the following informalities:

As for claims 10, 16, 17, 18, 24, 25, 30, 46 and 47, acronyms (such as USB in claim 10) should not be used to abbreviate key phrases until they are explicitly defined previously within the claim, or in a claim to which it depends. An example of an accepted correction would be "Universal Serial Bus (USB)".

As for claim 23, the phrase "said respective operating systems" lacks antecedent basis as this phrase has not specifically been set forth previously within the claims. Please consider the following as a possible alternative: "The computer system of claim 22, wherein each respective operating system stored in each said respective second memory is different".

Claims 11-15, 19-22, 26-29, 31-45 and 48-50 are further objected to as being dependant on one of the nine aforementioned claims.

Appropriate correction is required.

Drawings

2. The drawings received on 07/03/2003 are deemed acceptable by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6, 18-23, 39-41, 44, 47 and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki (US Patent 6,601,139 B1).

As for claims 1 and 18, Suzuki teaches a memory device (and computer system) comprising:

a processor (Fig. 3, element 11);

a bus (Fig. 3, the bus connects the processor to the removable media device, along with the other components illustrated in the figure) permanently operationally connected to the processor;

at least one memory device including:

a first, directly executable memory for storing boot code of a computer (Fig. 5, ROM area (elements 2a1-2a5). Note in col. 8, lines 17-28 – the boot area is stored directly after the lead-in area, which is stored on the ROM. Referring to figure 4, the ROM area is comprised of the lead-in area and the pre-mastered area. The latter contains the boot area as shown in Fig. 4).

a second memory (Fig. 5, RAM area (element 2b); and

a respective connector for reversible operationally connecting said two memories and said bus to said computer (The removable media device (Fig. 3 element 10) is connected to the system bus via a single interface – col. 7, lines 7-20) in

order to exchange signals between the processor and the first and second memories. Also note in col. 7, lines 18-20 – Suzuki discusses his media device as including a PCMIA card. A PCMIA card's interface is inherently reversible.

Conversely, each of the ROM areas as shown in Fig. 5 could be considered separate memories (i.e. ROM area #1 is the first memory, and ROM area #2 is the second memory).

As for claim 2, Suzuki teaches the device of claim 1, wherein said operational connection is reversible (col. 7, lines 18-20 – Suzuki discusses a PCMIA card (a PCMIA card interface is inherently reversible)).

As for claim 3, Suzuki teaches the device of claim 1, wherein said operational connection is permanent (col. 7, lines 18-20 – Suzuki discusses a PCMIA card which contains a permanent connection).

As for claim 4, Suzuki teaches the device of claim 1, wherein said first memory is a read-only memory (Fig. 5, elements 2a1-2a5).

As for claim 5, Suzuki teaches the device of claim 1, wherein said second memory is for storing an operating system of said computer (ROM area #2 stores the OS – col. 9. lines 45-48).

As for claim 6, Suzuki teaches the device of claim 1, wherein said second memory is a magnetic disk memory (the removable media can include a magnetic disk – col. 16, lines 15-22).

As for claim 19, Suzuki discloses the computer system of claim 18, wherein the computer system lacks a BIOS having a permanent operational connection

to said bus (Fig. 3 discloses a basic media access program, however no BIOS is contained within the computer (element 1)).

As for claim 20, Suzuki discloses the computer system of claim 18, wherein, in each said at least one memory device; said respective first memory is for storing respective boot code for the computer system. Note in col. 8, lines 17-28 – the boot area is stored directly after the lead-in area, which is stored on the ROM. Referring to figure 4, the ROM area is comprised of the lead-in area and the pre-mastered area. The latter contains the boot area as shown in Fig. 4).

As for claim 21, Suzuki discloses the computer system of claim 18, wherein, in each said at least one memory
device, said respective second memory is for storing a respective operating system for the computer system (ROM area #2 stores the OS – col. 9. lines 45-48).

As for claim 22, Suzuki discloses the computer system of claim 21, comprising a plurality of said memory devices (Fig. 1, elements 21-24 disclose multiple removable media devices).

As for claim 23, Suzuki discloses the computer system of claim 22, wherein all said respective operating systems are different (col. 10, lines 55-64) – various different OS can be stored on different disks.

As for claim 39, Suzuki discloses a method of operating a computer, comprising the steps of:

(a) providing at least one memory device including:

(i) a respective first, directly executable memory (as discussed in the rejection of claims 1 and 18 above), and

(ii) a respective second memory (as discussed in the rejection of claims 1 and 18 above);

(b) for each said at least one memory device, storing boot code of the computer in said respective first memory (as discussed in claims 1 and 18 above);

(c) operationally connecting one of said at least one memory device to the computer (as discussed in the rejection of claims 1 and 18 above); and

(d) executing said boot code that is stored in said respective first memory of said one memory device, by the computer (Fig. 5, ROM area (elements 2a1-2a5). Note in col. 8, lines 17-28 – the boot area is stored directly after the lead-in area, which is stored on the ROM. Referring to figure 4, the ROM area is comprised of the lead-in area and the pre-mastered area. The latter contains the boot area as shown in Fig. 4).

As for claim 40, Suzuki discloses the method of claim 39, wherein said operational connection is reversible (col. 7, lines 18-20 – Suzuki discusses a PCMIA card (a PCMIA card interface is inherently reversible)).

As for claim 41, Suzuki teaches the method of claim 39, further comprising the step of:

for each said at least one memory device, storing an operating system of the computer in said respective second memory (ROM area #2 stores the OS – col. 9. lines 45-48); and

wherein said executing of said boot code includes copying said operating system from said respective second memory of said one memory device to the computer (col. 12, lines 3-7 – The OS is loaded from the disk to the main memory of the computer).

As for claim 44, Suzuki teaches the method of claim 41, wherein a plurality of said memory devices are provided, each said memory device having a respective operating system of the computer stored in said second memory thereof; and wherein all said respective operating systems are different (col. 10, lines 55-64) – various different OS can be stored on different disks.

As for claim 47, Suzuki teaches a method of securing a computer, comprising the steps of:

omitting a BIOS from the computer (Fig. 3 discloses a basic media access program, however no BIOS is contained within the computer (element 1));

providing a memory device, separate from the computer, said memory device including a first, directly executable memory (as discussed in the rejection of claims 1 and 18 above);

storing boot code of the computer in said first memory (as discussed in the rejection of claims 1 and 18 above); and

reversibly operationally connecting said memory device to the computer (as discussed in the rejection of claims 1 and 18 above).

As for claim 50, Suzuki teaches the method of claim 47, wherein said memory device further includes a second memory;

wherein the method further comprises the step of:

storing an operating system of the computer in said second memory (ROM area #2 stores the OS – col. 9. lines 45-48); and

wherein said executing of said boot code includes copying said operating system from said second memory to the computer (col. 12, lines 3-7 – The OS is loaded from the disk to the main memory of the computer).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7, 45, and 48-49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in further view of Solhjell (US Patent 5,542,082).

As for claim 7, though Suzuki teaches all of the limitations of claim 1, he fails to specifically teach the second memory as being comprised of a flash memory. Solhjell however discloses a data storage system connected to a host computer capable of storing a boot program, which does include a flash memory (Fig. 3, element 21). It would have been obvious to one of ordinary skill in the art

at the time of the invention for Suzuki to have had utilized FLASH memory instead of ROM in the removable media device. Suzuki stores the BIOS in the ROM, therefore he would benefit from Solhjell's system by making it possible to upgrade the BIOS in the field using flash EEPROM as taught by Solhjell in col. 2, lines 33-34.

As for claims 45, 48, and 49 though Suzuki teaches all of the limitations of claim 39 and 47, he fails to teach executing said boot code directly from the first memory, by the computer. Solhjell however does teach this limitation in his disclosure (col. 3, lines 65-67 – the boot program may be started in the RAM memory (for the purposes discussed here, the first memory) by the host). It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to further include the option of the host executing the boot code stored in the first memory of Suzuki's system. By doing so, Suzuki would benefit by allowing the storage system to directly update the control program with little or no control from the host system as taught by Sulhjell in col. 3, lines 3-9.

5. Claims 8-10, 24-27, 29, 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in further view of Ma (US PG Publication 2004/0042735 A1).

As for claims 8 and 24, though Suzuki teaches all the limitations of claims 1 and 18, he fails to include a USB controller for supporting communication between the second memory and the computer. Ma however teaches benefits of implementing a USB connection between two electronic apparatuses (paragraph 0002, lines 1-5). It

would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to further include a USB controller as a means of interfacing the computer system. By doing so, Suzuki would benefit by realizing faster communication between the removable media device and the computer system as compared to other standard interface techniques. Ma discusses the benefits of USB in his teachings (in paragraph 004, lines 1-8, Ma discusses the advantages of using USB over other standard techniques with respect to signal transmission speed).

As for claims 9 and 10, though Suzuki discloses storing the read-only driver in the first memory (ROM area #2 stores the device drivers – col. 9, lines 45-47), he does not specifically include USB as the driver type in his teachings. As discussed with respect to the rejection of claim 8 (and the reasons for rejection set forth in that claim), it would have been obvious for Suzuki to further include USB as a type of driver stored in the memory in further view of the teachings of Ma.

As for claim 25, though Suzuki discloses a computer peripheral device comprising:

a first component (Fig. 5, ROM elements 2a1-2a5);

a second component separate from said first component (Fig. 5, RAM element 2b). Note that even though the example in Fig. 5 illustrates one disk, Suzuki further teaches the use of separate ROM and RAM ICs to accomplish the same purpose as the disk in Fig. 5. For example, the removable media device as shown in Fig. 5 may be replaced with a hybrid type medium containing separate ROM and RAM ICs (col. 16, lines 15-

27). In this embodiment, the media would include two distinct ICs (one ROM, one RAM), which would then be implemented in a similar fashion as discussed previously with the single disk as illustrated in Fig. 5.;

a connector for operationally connecting said first and second components to a computer (the removable media device (Fig. 3 element 10 is connected to the system bus via a single interface – col. 7, lines 7-20));

he fails to include a USB controller for supporting communication between the first component and the computer. Ma however teaches benefits of implementing a USB connection between two electronic apparatuses (paragraph 0002, lines 1-5).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to further include a USB controller as a means of interfacing the computer system. By doing so, Suzuki would benefit by realizing faster communication between the removable media device and the computer system as compared to other standard interface techniques. The benefits of USB interfaces are taught by Ma and discussed in the rejection of claims 8 and 24 above.

As for claims 26 and 27, Suzuki teaches the first component as being magnetic memory (col. 16, lines 15-22).

As for claims 29 and 31, Suzuki teaches the second component as a directly executable read-only memory for storing boot code (Fig. 5, ROM area (elements 2a1-2a5). Note in col. 9, lines 29-33 – the boot area is stored within the

ROM area as shown in Fig. 5. The system loader program within the boot area executes the loading software).

As for claim 32, Suzuki teaches the device of claim 29 wherein operational connection is reversible col. 7, lines 18-20 – Suzuki discusses a PCMIA card (a PCMIA card interface is inherently reversible).

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in further view of Ma in further view of Solhjell.

As for claim 28, though the combined teachings of Suzuki, and Ma meet all of the limitations of claim 26, they fail to teach the memory as being comprised of flash memory. Solhjell however discloses a data storage system connected to a host computer capable of storing a boot program, which does include a flash memory (Fig. 3, element 21). It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to have had utilized FLASH memory instead of ROM in the removable media device. Suzuki stores the BIOS in the ROM, therefore he would benefit from Solhjell's system by making it possible to upgrade the BIOS in the field using flash EEPROM as taught by Solhjell in col. 2, lines 33-34.

7. Claims 11-13, 33-35 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in further view of Gene (US Patent 6,757,751 B1).

As for claims 11 and 33, though Suzuki teaches all of the limitations of claim 1 and 25, he fails to teach the removable media device's connector as comprised of a plurality of pins as disclosed by applicant. Gene however, teaches a high-speed, multiple-bank, stacked memory module, which meets all the limitations of claims 11 and 25 including:

a first plurality of pins for supporting communication between said first memory and said computer; and a second plurality of pins for supporting communication between said second memory and said computer (Fig. 3, multiple memory modules are illustrated each connected to the CPU, each with unique I/O leads – Col. 7, line 65 through col. 8 line 6).

As for claims 12, and 34, Gene discloses the first and second plurality of pins as being separate (Fig. 3, multiple memory modules are illustrated, each connected to the CPU with separate I/O leads – Col. 7, line 65 through col. 8 line 6)

As for claims 13 and 35, Gene discloses at least one pin as being shared between each of the memory units (Fig. 3, the clock signal is common to each memory unit, likewise in col.8, lines 1-13 Gene discusses shared control and I/Os between two different banks).

As for claim 38, Gene discloses the second plurality of pins as including separate pins for address and data signals (col. 8, lines 5-13).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to implement Gene's system on the example Suzuki gives in col. 16 lines 15-25 of a removable media device being implemented in the form of a

memory card. By doing so, Suzuki would benefit from Gene's system by exploiting the use of shared pins for each of the memory units, which in turn will minimize the number of I/O connections needed for the interface, which in turn will decrease the cost and improve the yield of the memory used for the media card as taught by Gene (col. 2, lines 5-15).

8. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in further view of Ma in further view of Zimmer et al. (hereinafter Zimmer) US PG Publication 2005/0021968 A1.

Though the combined teachings of Suzuki, and Ma meet all of the limitations of claim 29, they fail to teach the connector as supporting a LPC protocol for the second component. Zimmer however teaches a method for performing a trusted BIOS update with the use of an LPC protocol, which can be launched from a removable media drive (paragraph 0023, lines 1-7). It would have been obvious to one of ordineary skill in the art at the time of the invention for Suzuki to further include Zimmer's method of securing a BIOS update via the LPC protocol. By doing so, Suzuki would benefit from Zimmer's verification and authentication of the boot (or BIOS) information stored on the removable media device, which in turn would prevent the problems associated with receiving un-authentic or corrupt boot images (paragraph 003, lines 5-13).

Allowable Subject Matter

9. Claims 14-17, 36-37, 42-43 and 46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

As for claims 14 and 36, Suzuki fails to teach a switch for alternately connecting the first and second memory to the computer via at least one shared pin.

As for claim 15, Suzuki fails to teach separate access protocols for each of the two groupings of pins.

Claims 16-17 further limit claim 15 therefore they are deemed allowable.

As for claim 37, Suzuki fails to teach the communication as multiplexing the second plurality of pins between the second component and the computer.

As for claim 42, though Suzuki teaches all of the limitations claim 41 wherein for each said at least one memory device, said boot code includes driver code for said respective second memory (col. 9, lines 45-47), he fails to teach wherein said copying of said operating system from said respective second memory of said one memory device to the computer is effected by executing at least a portion of said driver code.

As for claim 43, though Suzuki teaches all of the limitations of this claim (col. 9, lines 45-47), it further limits claim 42, therefore it too is deemed allowable.

As for claim 46, Suzuki fails to teach wherein said executing of said boot code is effected by steps including: (i) executing only a portion of said boot code directly from said first memory; (ii) copying a remainder of said boot code to a RAM; and (iii) executing said reminder of said boot code from said RAM.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lee et al. (US PG Publication 2003/0172261 A1) disclose a system boot using NAND flash memory.

Thomas et al. (US PG Publication 2004/0083473 A1) teaches a self-contained application disk for automatically launching application software or starting devices and peripherals.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

Reginald G. Bragdon

REGINALD G. BRAGDON
PRIMARY EXAMINER